

ABSTRACT

A processor configuration for processing multi-precision shift instructions is provided.

The multi-precision shift instructions are executed following a previous shift instruction of the same increment, such as a logical or arithmetic left or right shift operation. The first shift

5 instruction shifts a first memory word by the shift increment and stores this shifted value into memory. The second, and any subsequent, multi-precision shift instruction shifts the next memory word by the shift increment and concatenates the bits shifted out of the previously shifted memory word into bit positions of the memory word presently being shifted. This concatenated value is then stored back to memory and forms another part of the multi-precision
10 shifted value.